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FROM: Rob Sullivan RN6-30

DATE: August 15, 1995

SUBJECT: MS/Intel IP & EM Discussion with Maritz 8/15

Summary

A very positive and pragmatic meeting given our Unix API press release today (Maritz barely commented on this) and the long history of contention and posturing in this space. Re MMx Maritz pushed hard for a ceiling bounding our "reasonable terms" negotiation with AMD and others on MMx; we insisted that Maritz trust our good faith commit.

Re EM, we defined a two-phased approach:

- Up front, an agreement not to encumber each other or our customers for combinations of Intel/HP cpus and MS OS software which are not infringing but for support of the EM architecture. This level of agreement (which seems to us like belt & suspenders along the lines of patent exhaustion) along with philosophical agreement on the intention to negotiate to the second phase (below) would leave MS comfortable to accept EM disclosure, to begin to give feedback on EM, and to work through the definition of "open" which would be addressed in the second phase.
- Second, MS established that a mutual and reciprocal commitment to the EM ISA as an "open" interface, unencumbered for independent support/implementation by other OSVs/cpu vendors, would make MS comfortable to invest aggressively in EM products including an EM timeframe Cairo product. Such an agreement should enable competition "within layers" while respecting IP investments by Intel/HP and MS- "like x86 today", with multiple OSVs and independent implementations of x86 cpus.

Maritz made it clear that the commitment to "open" is not a pre-requisite for MS support. but that to the degree that we can define the "open" line MS would be willing to radically accelerate their productization investment for EM. The focus for the second phase should be pre-plan'96 for both companies on the assumption that '96 investments would be affected by the outcome. We should target Q4 for closure here.

Gates may require that the mutual "no-338s for EM" part of "open" be established up-front, i.e. to enable the immediate EM engagement. Intel has not reached consensus on "open-ness" for EM. Yu & Maritz committed to close in the coming week on both of these issues.

Up Front MMx Discussion

- Maritz again expressed desire for Intel to cap our "reasonable terms" expectations of imitators desiring "necessary" MMx implementation patents. We refused but fell back on our verbal commitment to make MMx "open" and to entertain negotiation with imitators on "necessary" implementation patents for reasonable terms.
- MS willingness to support MMx in tools, OS, and apps is not conditioned upon our willingness to license MMx; MS enthusiasm and urgency for investing in MMx support is.
- Our initial engagement with MS tools and OS teams has met a non-committal response from MS. Maritz committed to a complete checkpoint in mid-September on MMx: MS will have some indication from imitators as to their comfort level with MMx (key indicator will be AMD warming to MMx instead of advocating their own nsp extension to MS) and they'll have proposals from MS developers re the cost/benefits of MMx investment in specific areas.
- In the afternoon session which followed, Silverberg seemed eager to get started on MMx. Perhaps he's internalized that MMx is the wagon that he can hitch the '96 Windows product to to win compelling benefit and high adoption.
- Maritz did ask for a "written", i.e. not email, note from Yu to affirm our intent on MMx. A signed letter with the email already sent included verbatim is all Maritz is asking for "for the record". **AR: Yu in next few days.**

Microsoft & Intel Positions & 'Philosophy'

- MS makes significant investment in s/w and desires safety and comfort around those investments. Safety and comfort means an IP position sufficient to ensure continued healthy competition in non-MS layers of the horizontal model, independent of the uncertainties of changing Intel/MS business objective alignment in the future. In lieu of a stable IP environment (comfort) MS' only option is hedge investments in alternatives (RISC) to ensure continued competition which protects their return on investment in technology like NT, Office, etc. They assume we value such comfort regarding the OS layer as well.
- MS proposes a "clean contract", an interface line between MS & Intel's dependent core investments, across which we won't encumber each other's products: specifically Intel CPU (*not* cache, chipset, or other hardware beyond cpu) and MS OS (*not* apps or h/w products).

- Suppose an imitator independently developed an EM architecture cpu but found that a certain Intel EM patent to be "necessary" for ISA compatible completion of the implementation. Intel would agree to license that patent "for reasonable terms".
- Suppose an OSV were to conclude that an EM feature could not be supported (again: "necessary") without infringing an MS patent MS would agree to license the patent "for reasonable terms" in the manner noted above.
- An EM agreement would *not* seek to redress latent (e.g. pre-EM) patent liabilities between OSVs or cpu vendors. Conceptually "not infringing but for support of the EM ISA" limits the scope of these patents.

Levels 1, 2, & 3

After discussion and consideration of levels of "open-ness" we identified three levels of IP commitment. MS is tentatively willing to begin engagement on EM- to kick off EAS 2.0 evaluation and feedback and to enable enlightened discussion on the latter two 'levels' based on agreement on Level 1 and on a documented mutual intention (an LOI) assuring #2 & #3 as a direction for attempted convergence.

In lieu of agreement on #2 & #3, MS would (worst case) not productize on EM at all, and we would not have rights to MS Suggestions incorporated in our EM ISA specification. Best case, MS would productize on EM without the commitment or urgency that would be enabled by closure on #2 & #3 and we likely would not get EM NT in '97 or '98 timeframe.

Stork thinks we'll do #1 and will never do #2 or #3. This is the basis for his advocacy to Maritz for requiring #3 commit "up front", he also believes Gates will require this. Maritz scoffed and said he'd work this with Gates directly.

Three levels:

1. *"Exhaustion" assurance for Intel/HP and MS & our mutual customers.*

   Apparently our legal teams agree that patent exhaustion ensures that we won't sue our mutual customers for combining MS OS Software on Intel/HP processors (each not infringing but for support of EM ISA). MS is concerned that patent exhaustion may not be an assured doctrine in other countries, etc. and wants to codify this with Intel.

   Exhaustion offers no assurance that we won't sue each other making/selling complementary products. MS would like to address this also in level 1; again, only for combinations of Intel/HP cpu + MS OS products that are not infringing "but for" support of EM.

2. *Symmetrical "open-ness" around the ISA interface line that enables reasonable intra-layer competition.*

   Intel/HP and MS would each agree to license others, on reasonable terms, for IP necessary to implement EM ISA compatibility in cpus or OS Software.

   This does not mean that we'd license whole implementations or, for instance, circuit patents or bus patents which are not necessary for a "clean

room" type implementation of the EM architecture.

3. *Commitment not to sue our collective customers (in the chain of distribution) for selling/using combinations of either Intel/HP cpus or MS OS software which are not infringing but for support of EM.*

   This level would cover combination patent rights around EM in the manner of today's P6 ("CPU Feature Agreement") agreement except with complete symmetry about the EM ISA axis. Hence, MS would commit not to sue Intel or Intel customers also.

   "No '338s for EM" is the essence, the combination patents are those infringed by combinations of MS OS and Intel/HP cpus. The P6 agreement benefits MS & MS customers- the agreement we discussed would benefit Intel/HP & our customers also.

   Rights to be granted only for systems which are otherwise "legal". This is new wording, added by MS now that the rights are reciprocal. Its assumed that they want to exclude OSs which incorporate unlicensed MS technology (outside of the EM scope?). We need to understand MS intentions here and to understand what the reciprocal case would be for these rights.

Yu noted that we'll need to close internally on "MMx like" openness for EM. Maritz noted that he'd need Gates' buy-in to allow our engagement to begin in lieu of a signed & closed Level #3 agreement.

Next Steps: EM negotiation ARs

1. **Draft LOI for legal review Friday 8/18, LOI in Maritz's hands by Wed 8/23. Salvador drafting, Yu/Sullivan/legal to review.**
2. **Yu to close with Grove/ESM re "open" strategy for EM, negotiation walk points.**
3. **Close Maritz on regular process to pace the negotiation (establish in LOI?). Yu to Maritz, 8/23.**
4. **Determine drafting and negotiation approach: incremental changes to MS 7/31 draft or clean slate? Salvador/Sullivan/Moradzadeh meeting 8/22 to close, review with Yu.**

Issue Detail: Emulators

- Emulators are sometimes good (Floating Point on 486SX is classic case) and there are probably analogs in EM for these. Its probably too early to commit these away up front in our view, which MS accepted.
- We agreed that our agreement need not enable parties to enable imitators or OS competitors to side-step the need to license "necessary" patents from respective parties. Hence, MS would not ship emulator code to complete an otherwise non-

infringing imitator cpu implementation without licensing the "necessary" patent from Intel/HP.

- Emulators are "implementation" code and fall on the Intel/HP side of the ISA line as implementation of the architecture. As such MS would expect that "IP necessary" to implement would be available on reasonable terms... as described in level 2.

Issue Detail: Compilers

- Maritz's perception is that the Intel/MS compiler agreement negotiation that he suspended earlier this year was "way off". Maritz recognizes that key architecture implementation trade secrets and key Intel/HP IP is embodied in an EM compiler.
- MS expects that they'd be able to productize a "reasonable" compiler for an "open" cpu architecture.
- Maritz does not yet comprehend our intention to completely separate the ISA (Architecture) definition for EM from our microarchitecture and implementation plans. We expect that 30-40% of the ISPEC performance of Merced will be due to gains in the compiler; to the degree that this is a significant basis for competition for us we don't want to lose control of it.

Given this it is a positive that Maritz agreed to table these issues for the Compiler engagement/licensing discussions with Heinen. Maritz expected that we could re-engage on these discussions after the "level 1" LOI and agreement is established. We'll need to review our compiler engagement POR/strategy once again before we begin. **AR: Sullivan/Salvador with Wirt/Fu et al in next two weeks.**

The Whiteboard- framing the 3 levels with minimum words.

This is what was on the whiteboard in Maritz's office by the end of the meeting...

1. MS can write/sell SW on Intel EM proc.
   Intel can make/sell EMuP using WinOS
   + customers
2. Intel plans to make EM "open" at ISA
   level - details TBD
3. If EM h/w can legally be made/sold, then Intel won't sue combos MSOS/EMhw
   If other OS can legally be made/sold then MS won't sue combos w/EM

P6 & P6C Positioning Discussion

- MS greatly admires our multiple segment market model and the ability to introduce new products at higher and higher ASPs- they've been studying our traditional waterfall vs. segment roadmap foils. With Windows '9x and a single 'segment' they end up red-X'ing each generation of the OS completely with next and they are pressured to have low ASPs to encourage total adoption of the new generation.
- Its wrong to ask "when will Win '9x be replaced completely by NT". In reality, its "when will the Win '9x product family be based substantially on NT technology". They plan to position multiple products into their market segmentation and over time these products will use more and more of the same technology.
- Associating NT with one Intel cpu and Windows '9x with another only makes sense in a particular and narrow time frame. It'll be better to align our segmentation and

product-to-segment distribution expectations and to develop a natural affinity for volume products with Win '9x, for high-end products with Cairo/NT for instance. This alignment & affinity intention could impact our naming and intro positioning for both MMx and for P6/P6C.

MS is eager to continue these discussions- Silverberg & Maritz both expressed interest in this area. Everett agreed to sync up before our quarterly geography roadmap updates and to continue the conversation on 9/15. **AR: Everett, pre-quarterly OEM updates,** and **AR: Everett for 9/15 MS meeting.**

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